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     FILE 'USPATFULL, CAPLUS' ENTERED AT 11:28:51 ON 23 SEP 2002
L1          9860 S LOW (6W) DIELECTRIC CONSTANT
L2          3051 S L1 AND PLASMA
L3            98 S L2 AND NITRAT?
L4            18 S L3 AND SILICON CARBIDE

=> d pn l3 total

L3   ANSWER 1 OF 98  USPATFULL
PI     US 2002127843       A1   20020912

L3   ANSWER 2 OF 98  USPATFULL
PI     US 2002127842       A1   20020912

L3   ANSWER 3 OF 98  USPATFULL
PI     US 6447838          B1   20020910

L3   ANSWER 4 OF 98  USPATFULL
PI     US 6447695          B1   20020910

L3   ANSWER 5 OF 98  USPATFULL
PI     US 2002123158       A1   20020905

L3   ANSWER 6 OF 98  USPATFULL
PI     US 2002119651       A1   20020829

L3   ANSWER 7 OF 98  USPATFULL
PI     US 2002117758       A1   20020829

L3   ANSWER 8 OF 98  USPATFULL
PI     US 6441489          B1   20020827

L3   ANSWER 9 OF 98  USPATFULL
PI     US 6440864          B1   20020827

L3   ANSWER 10 OF 98  USPATFULL
PI     US 2002113271       A1   20020822

L3   ANSWER 11 OF 98  USPATFULL
PI     US 6435944          B1   20020820

L3   ANSWER 12 OF 98  USPATFULL
PI     US 2002111026       A1   20020815

L3   ANSWER 13 OF 98  USPATFULL
PI     US 2002108861       A1   20020815

L3   ANSWER 14 OF 98  USPATFULL
PI     US 2002105612       A1   20020808

L3   ANSWER 15 OF 98  USPATFULL
PI     US 2002105611       A1   20020808

L3   ANSWER 16 OF 98  USPATFULL
PI     US 2002098701       A1   20020725

L3   ANSWER 17 OF 98  USPATFULL
PI     US 6423248          B1   20020723
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L3   ANSWER 18 OF 98  USPATFULL
PI    US 6423148          B1   20020723

L3   ANSWER 19 OF 98  USPATFULL
PI    US 2002093290       A1   20020718

L3   ANSWER 20 OF 98  USPATFULL
PI    US 2002092827       A1   20020718

L3   ANSWER 21 OF 98  USPATFULL
PI    US 2002077035       A1   20020620

L3   ANSWER 22 OF 98  USPATFULL
PI    US 2002076933       A1   20020620

L3   ANSWER 23 OF 98  USPATFULL
PI    US 2002076495       A1   20020620

L3   ANSWER 24 OF 98  USPATFULL
PI    US 6380687          B1   20020430

L3   ANSWER 25 OF 98  USPATFULL
PI    US 6380007          B1   20020430

L3   ANSWER 26 OF 98  USPATFULL
PI    US 2002048959       A1   20020425

L3   ANSWER 27 OF 98  USPATFULL
PI    US 2002048531       A1   20020425

L3   ANSWER 28 OF 98  USPATFULL
PI    US 6372286          B1   20020416

L3   ANSWER 29 OF 98  USPATFULL
PI    US 2002042193       A1   20020411

L3   ANSWER 30 OF 98  USPATFULL
PI    US 6368665          B1   20020409

L3   ANSWER 31 OF 98  USPATFULL
PI    US 2002037481       A1   20020328

L3   ANSWER 32 OF 98  USPATFULL
PI    US 6361712          B1   20020326

L3   ANSWER 33 OF 98  USPATFULL
PI    US 6360562          B1   20020326

L3   ANSWER 34 OF 98  USPATFULL
PI    US 2002022370       A1   20020221
      US 6451697          B2   20020917

L3   ANSWER 35 OF 98  USPATFULL
PI    US 6348395          B1   20020219

L3   ANSWER 36 OF 98  USPATFULL
PI    US 2002016085       A1   20020207
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L3   ANSWER 37 OF 98  USPATFULL
PI     US 2002016060      A1   20020207
       US 6420269         B2   20020716

L3   ANSWER 38 OF 98  USPATFULL
PI     US 2002011983      A1   20020131

L3   ANSWER 39 OF 98  USPATFULL
PI     US 2001054728      A1   20011227

L3   ANSWER 40 OF 98  USPATFULL
PI     US 6323300         B1   20011127
       WO 9823664  19980604

L3   ANSWER 41 OF 98  USPATFULL
PI     US 2001044201      A1   20011122
       US 6417116         B2   20020709

L3   ANSWER 42 OF 98  USPATFULL
PI     US 2001037821      A1   20011108

L3   ANSWER 43 OF 98  USPATFULL
PI     US 2001033026      A1   20011025

L3   ANSWER 44 OF 98  USPATFULL
PI     US 2001032829      A1   20011025

L3   ANSWER 45 OF 98  USPATFULL
PI     US 2001030367      A1   20011018

L3   ANSWER 46 OF 98  USPATFULL
PI     US 2001030366      A1   20011018

L3   ANSWER 47 OF 98  USPATFULL
PI     US 2001029104      A1   20011011
       US 6444583         B2   20020903

L3   ANSWER 48 OF 98  USPATFULL
PI     US 6288188         B1   20010911

L3   ANSWER 49 OF 98  USPATFULL
PI     US 6285048         B1   20010904

L3   ANSWER 50 OF 98  USPATFULL
PI     US 6277726         B1   20010821

L3   ANSWER 51 OF 98  USPATFULL
PI     US 6271818         B1   20010807

L3   ANSWER 52 OF 98  USPATFULL
PI     US 2001010573      A1   20010802
       US 6392730         B2   20020521

L3   ANSWER 53 OF 98  USPATFULL
PI     US 2001009447      A1   20010726
       US 6388725         B2   20020514
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L3 ANSWER 54 OF 98 USPATFULL
PI US 6265309 B1 20010724

L3 ANSWER 55 OF 98 USPATFULL
PI US 2001008828 A1 20010719

L3 ANSWER 56 OF 98 USPATFULL
PI US 2001007795 A1 20010712

L3 ANSWER 57 OF 98 USPATFULL
PI US 6249039 B1 20010619

L3 ANSWER 58 OF 98 USPATFULL
PI US 6245663 B1 20010612

L3 ANSWER 59 OF 98 USPATFULL
PI US 6208399 B1 20010327
WO 9847044 19981022

L3 ANSWER 60 OF 98 USPATFULL
PI US 6187427 B1 20010213

L3 ANSWER 61 OF 98 USPATFULL
PI US 6183934 B1 20010206

L3 ANSWER 62 OF 98 USPATFULL
PI US 6183933 B1 20010206

L3 ANSWER 63 OF 98 USPATFULL
PI US 6159654 20001212

L3 ANSWER 64 OF 98 USPATFULL
PI US 6155726 20001205

L3 ANSWER 65 OF 98 USPATFULL
PI US 6147667 20001114

L3 ANSWER 66 OF 98 USPATFULL
PI US 6083661 20000704

L3 ANSWER 67 OF 98 USPATFULL
PI US 6080592 20000627

L3 ANSWER 68 OF 98 USPATFULL
PI US 6001517 19991214

L3 ANSWER 69 OF 98 USPATFULL
PI US 5981972 19991109

L3 ANSWER 70 OF 98 USPATFULL
PI US 5965679 19991012

L3 ANSWER 71 OF 98 USPATFULL
PI US 5965202 19991012

L3 ANSWER 72 OF 98 USPATFULL
PI US 5928791 19990727

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L3   ANSWER 73 OF 98  USPATFULL
PI     US 5830563               19981103

L3   ANSWER 74 OF 98  USPATFULL
PI     US 5760854               19980602

L3   ANSWER 75 OF 98  USPATFULL
PI     US 5723266               19980303

L3   ANSWER 76 OF 98  USPATFULL
PI     US 5671027               19970923

L3   ANSWER 77 OF 98  USPATFULL
PI     US 5668379               19970916

L3   ANSWER 78 OF 98  USPATFULL
PI     US 5610738               19970311

L3   ANSWER 79 OF 98  USPATFULL
PI     US 5585450               19961217

L3   ANSWER 80 OF 98  USPATFULL
PI     US 5519234               19960521

L3   ANSWER 81 OF 98  USPATFULL
PI     US 5480048               19960102

L3   ANSWER 82 OF 98  USPATFULL
PI     US 5468679               19951121

L3   ANSWER 83 OF 98  USPATFULL
PI     US 5423285               19950613

L3   ANSWER 84 OF 98  USPATFULL
PI     US 5402254               19950328

L3   ANSWER 85 OF 98  USPATFULL
PI     US 5380612               19950110

L3   ANSWER 86 OF 98  USPATFULL
PI     US 5308888               19940503

L3   ANSWER 87 OF 98  USPATFULL
PI     US 5190808               19930302

L3   ANSWER 88 OF 98  USPATFULL
PI     US 5177670               19930105

L3   ANSWER 89 OF 98  USPATFULL
PI     US 5120339               19920609

L3   ANSWER 90 OF 98  USPATFULL
PI     US 5071701               19911210

L3   ANSWER 91 OF 98  USPATFULL
PI     US 5042895               19910827

L3   ANSWER 92 OF 98  USPATFULL
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PI US 5011804 19910430

L3 ANSWER 93 OF 98 USPATFULL
PI US 4988413 19910129

L3 ANSWER 94 OF 98 USPATFULL
PI US 4917451 19900417

L3 ANSWER 95 OF 98 USPATFULL
PI US 4783368 19881108

L3 ANSWER 96 OF 98 USPATFULL
PI US 4720419 19880119

L3 ANSWER 97 OF 98 USPATFULL
PI US 4077782 19780307

L3 ANSWER 98 OF 98 CAPLUS COPYRIGHT 2002 ACS

	PATENT NO.	KIND	DATE
PI	EP 1172845	A2	20020116
	US 2002016085	A1	20020207
	JP 2002176100	A2	20020621

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=> d his

     (FILE 'HOME' ENTERED AT 10:18:11 ON 23 SEP 2002)

     FILE 'USPATFULL, CAPLUS' ENTERED AT 10:18:25 ON 23 SEP 2002
L1             77 S SILICON CARBIDE AND NITRATION?
L2             17 S L1 AND PLASMA?
L3              2 S L2 AND CHAMBER

=> d pn l2 total

L2   ANSWER 1 OF 17  USPATFULL
PI     US 6313429          B1   20011106

L2   ANSWER 2 OF 17  USPATFULL
PI     US 2001036530       A1   20011101

L2   ANSWER 3 OF 17  USPATFULL
PI     US 5710334               19980120

L2   ANSWER 4 OF 17  USPATFULL
PI     US 5676752               19971014

L2   ANSWER 5 OF 17  USPATFULL
PI     US 5588994               19961231

L2   ANSWER 6 OF 17  USPATFULL
PI     US 5549747               19960827

L2   ANSWER 7 OF 17  USPATFULL
PI     US 5480965               19960102

L2   ANSWER 8 OF 17  USPATFULL
PI     US 5413952               19950509

L2   ANSWER 9 OF 17  USPATFULL
PI     US 5362682               19941108

L2   ANSWER 10 OF 17  USPATFULL
PI     US 5328549               19940712

L2   ANSWER 11 OF 17  USPATFULL
PI     US 5273616               19931228

L2   ANSWER 12 OF 17  USPATFULL
PI     US 5217564               19930608

L2   ANSWER 13 OF 17  USPATFULL
PI     US 4837182               19890606

L2   ANSWER 14 OF 17  USPATFULL
PI     US 4816420               19890328

L2   ANSWER 15 OF 17  USPATFULL
PI     US 4783368               19881108

L2   ANSWER 16 OF 17  USPATFULL
PI     US 4727047               19880223
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L3	ANSWER 1 OF 2	USPATFULL	
PI	US 6313429	B1	20011106
L3	ANSWER 2 OF 2	USPATFULL	
PI	US 4783368		19881108

AN 2001:181216 USPATFULL|
TI Semiconductor integrated circuit device and fabrication method for semiconductor integrated circuit device|
IN Noguchi, Junji, Ome, Japan
Ohashi, Naohumi, Hannou, Japan
Saito, Tatsuyuki, Ome, Japan
PI US 2001030367 A1 20011018
AI US 2001-825946 A1 20010405 (9)
PRAI JP 2000-104015 20000405
DT Utility|
FS APPLICATION|
LREP ANTONELLI TERRY STOUT AND KRAUS, SUITE 1800, 1300 NORTH SEVENTEENTH STREET, ARLINGTON, VA, 22209|
CLMN Number of Claims: 45|
ECL Exemplary Claim: 1|
DRWN 78 Drawing Page(s)|

L2 ANSWER 27 OF 27 CAPLUS COPYRIGHT 2002 ACS
TI Method to reduce the moisture content in an organic **low dielectric constant** material
AB . . . absorbed by the org. low k layer, due to exposure to the environment, is then reduced via a high d. **plasma treatment**, performed in a **nitrogen** ambient. The redn. in moisture can be accomplished, even when the org. low k layer had been exposed to the. . .
AN 2002:444463 CAPLUS
DN 137:14454
TI Method to reduce the moisture content in an organic **low dielectric constant** material
IN Chang, Weng
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6403464	B1	20020611	US 1999-433053	19991103

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

AN 2000:160909 USPATFULL|
TI Process to improve adhesion of HSQ to underlying materials|
IN Chang, Chung-Long, Dou-Liu, Taiwan, Province of China
Jang, Syun-Ming, Hsin-Chu, Taiwan, Province of China
PA Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, Province of China (non-U.S. corporation)
PI US 6153512 20001128
AI US 1999-414922 19991012 (9)
DT Utility|
FS Granted|
EXNAM Primary Examiner: Tsai, Jey; Assistant Examiner: Gurley, Lynne|
LREP Saile, George O., Ackerman, Stephen B.|
CLMN Number of Claims: 17|
ECL Exemplary Claim: 1|
DRWN 5 Drawing Figure(s); 3 Drawing Page(s)|
LN.CNT 313|
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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AN      2001:103240  USPATFULL
TI      Semiconductor device and process for producing the same
IN      Yokoyama, Takashi, Tokyo, Japan
        Usami, Tatsuya, Tokyo, Japan
PA      NEC Corporation, Tokyo, Japan (non-U.S. corporation)
PI      US 6255732          B1   20010703
AI      US 1999-366517           19990803 (9)
PRAI    JP 1998-229708      19980814
DT      Utility
FS      GRANTED
EXNAM   Primary Examiner: Potter, Roy
LREP    Hayes, Soloway, Hennessey, Grossman & Hage PC
CLMN    Number of Claims: 14
ECL     Exemplary Claim: 1
DRWN    18 Drawing Figure(s); 9 Drawing Page(s)
LN.CNT 616
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
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L2 ANSWER 18 OF 27 USPATFULL

SUMM Fluorinated silica glass (FSG) is employed as a **low dielectric constant** (low-k) material for intermetal dielectric (IMD) layers for semiconductor technology of 0.18 .mu.m and beyond (i.e. smaller sizes). However, complications. . .

SUMM U.S. Pat. No. 6,054,379 to Yau et al. describes a method and apparatus for depositing a **low dielectric constant** film by reaction of an organo silane compound and an oxidizing gas.

DETD Second nitrogen gas/plasma treatment 32 preferably has the same composition as first nitrogen gas/**plasma treatment** 18. Second **nitrogen** gas/plasma treatment 32 treats at least the sidewalls 30 of via hole 26, to form sidewall capping layer 34, under. . .

AN 2001:147855 USPATFULL

TI IMD scheme by post-plasma treatment of FSG and TEOS oxide capping layer

IN Aug, Arthur Khoon Siah, Singapore, Singapore
Chen, Feng, Singapore, Singapore
Li, Qiong, Singapore, Singapore

PA Chartered Semiconductor Manufacturing Ltd., Singapore, Singapore (non-U.S. corporation)

PI US 6284644 B1 20010904

AI US 2000-684518 20001010 (9)

DT Utility

FS GRANTED

EXNAM Primary Examiner: Lebentritt, Michael

LREP Saile, George O., Pike, Rosemary L. S., Stanton, Stephen G.

CLMN Number of Claims: 44

ECL Exemplary Claim: 1

DRWN 8 Drawing Figure(s); 4 Drawing Page(s)

LN.CNT 583

AN   2001:223978 USPATFULL|
TI   Non-metallic barrier formations for copper damascene type
interconnects|
IN   Chooi, Simon, Singapore, Singapore
        Gupta, Subhash, Singapore, Singapore
        Zhou, Mei-Sheng, Singapore, Singapore
        Hong, Sangki, Singapore, Singapore
PA   CHARTERED SEMICONDUCTOR MANUFACTURING LTD. (non-U.S. corporation)
PI   US 2001049195   A1   20011206
AI   US 2001-925819   A1   20010810 (9)
RLI   Division of Ser. No. US 2000-512379, filed on 25 Feb 2000, GRANTED,
Pat.
        No. US 6284657
DT   Utility|
FS   APPLICATION|
LREP   George O. Saile, 20 McIntosh Drive, Poughkeepsie, NY, 12603|
CLMN   Number of Claims: 179|
ECL   Exemplary Claim: 1|
DRWN   5 Drawing Page(s)|
LN.CNT 1441|
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN	2002:1174 USPATFULL
TI	Method for forming a high-RI oxide film to reduce fluorine diffusion in HDP FSG process
IN	Wu, Shu-Li, Nan-Tao, TAIWAN, PROVINCE OF CHINA Jeng, Pei-Ren, Hsin-Chu, TAIWAN, PROVINCE OF CHINA
PA	Macronix International Co., Ltd., TAIWAN, PROVINCE OF CHINA (non-U.S. corporation)
PI	US 6335274 B1 20020101
AI	US 2000-714128 20001117 (9)
DT	Utility
FS	GRANTED
EXNAM	Primary Examiner: Nelms, David; Assistant Examiner: Le, Thao P.
CLMN	Number of Claims: 38

L2 ANSWER 9 OF 27 USPATFULL

TI Method to reduce the moisture content in an organic **low dielectric constant** material

AB . . . absorbed by the organic low k layer, due to exposure to the environment, is then reduced via a high density **plasma treatment**, performed in a **nitrogen** ambient. The reduction in moisture can be accomplished, even when the organic low k layer had been exposed to the. . .

SUMM . . . used to fabricate semiconductor devices, and more specifically to a method used to reduce the moisture content in an organic, **low dielectric constant**, (low k), layer, used to passivate metal interconnect structures.

SUMM . . . RC delays, when compared to counterparts fabricated with more resistive aluminum, or tungsten interconnect structures. In addition the use of **low dielectric constant**, (low k), materials. have allowed the capacitance value of RC delays to be significantly reduced. Inorganic spin on glass, (SOG),. . .

CLM What is claimed is:
1. A method of forming an organic **low dielectric constant**, (low k), layer, on a semiconductor substrate, featuring a final nitrogen procedure used to remove water from said organic low. . .

AN 2002:136891 USPATFULL|

TI Method to reduce the moisture content in an organic **low dielectric constant** material|

IN Chang, Weng, Taipei, TAIWAN, PROVINCE OF CHINA

PA Taiwan Semiconductor Manufacturing Company, Hsin-Chu, TAIWAN, PROVINCE OF CHINA (non-U.S. corporation)

PI US 6403464 B1 20020611

AI US 1999-433053 19991103 (9)

DT Utility|

FS GRANTED|

EXNAM Primary Examiner: Niebling, John F.; Assistant Examiner: Gurley, Lynne A.|

LREP Saile, George O., Ackerman, Stephen B.|

CLMN Number of Claims: 15|

ECL Exemplary Claim: 1|

DRWN 3 Drawing Figure(s); 1 Drawing Page(s)|

LN.CNT 271|

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

2   ANSWER 3 OF 27 USPATFULL

SUMM   The present invention relates generally to **low dielectric constant** materials used for the intermetal dielectric layer and more particularly to the use of fluorine containing **low dielectric constant** materials for intermetal dielectric layers for technologies of 0.18 .mu.m and below.

SUMM   . . . that the intermetal/interlevel dielectric layers (IMD and ILD layers) must be thinner. To reduce capacitive effects with the IMD/ILD materials, **low dielectric constant** (low-k) dielectric materials have been developed which have k values in the range of 3.2 down to 2.0. However, these. . .

SUMM   . . . deposited fluorinated silica glass (FSG) intermetal dielectric (IMD) films have been of high interest for submicron devices due to its **low dielectric constant** (k) and good gap-filling capability. However HDP FSG has several problems from a process integration aspect, such as fluorine out-gassing,. . .

DETD   Referring now to FIG. 9, therein is shown the structure of FIG. 8 after post-**plasma treatment** with an ammonia (NH.sub.3)-**nitrogen** (N.sub.2) gas mixture. This post-plasma treatment results in a fluorine-depleted region 32 in the FSG layer 18 around the via. . .

AN   2002:238937 USPATFULL
TI   Intermetal dielectric layer for integrated circuits
IN   Liu, Huang, Singapore, SINGAPORE
       Sudijono, John, Singapore, SINGAPORE
       Tan, Juan Boon, Singapore, SINGAPORE
       Goh, Edwin, Singapore, SINGAPORE
       Cuthbertson, Alan, Singapore, SINGAPORE
       Ang, Arthur, Singapore, SINGAPORE
       Chen, Feng, Singapore, SINGAPORE
       Li, Qiong, Singapore, SINGAPORE
       Chew, Peter, Singapore, SINGAPORE
PA   Chartered Semiconductor Manufacturing Ltd., Singapore, SINGAPORE (non-U.S. corporation)
       Lucent Technologies Inc., Allentown, PA, United States (U.S. corporation)
PI   US 6451687   B1   20020917
AI   US 2000-721898   20001124 (9)
DT   Utility
FS   GRANTED
EXNAM Primary Examiner: Quach, T. N.
LREP   Ishimaru, Mikio
CLMN   Number of Claims: 10
ECL   Exemplary Claim: 1
DRWN   10 Drawing Figure(s); 4 Drawing Page(s)
LN.CNT 270

L14 ANSWER 17 OF 20 USPATFULL

SUMM . . . gas for the non oxidative ambient, use may be made of a nitride
gas or an inert gas such as **argon** or **helium**.

SUMM The **plasma treatment** means is desired to treat a dielectric film containing one element selected from the group consisting of silicon dioxide, silicon nitride, **silicon carbide**, aluminum oxide, zirconium oxide, cupric oxide and tungsten oxide.

SUMM . . . of the treatment substrate containing silicon, the treatment substrate containing silicon and oxygen, and the treatment substrate containing silicon and **nitrogen** with the light.

DETD To the cooling pipe 28, a circulator 38 is provided. The circulator 38 circulates a coolant such as liquid **nitrogen** and cools the treatment substrate 26 rapidly. The lamp heater 27 used in combination with the cooling pipe 28 can. . .

CLM What is claimed is:
9. The measurement system according to claim 7, wherein the **plasma treatment** means treats a dielectric film containing one element selected from the group consisting of silicon dioxide, silicon nitride, **silicon carbide**, aluminum oxide, zirconium oxide, cupric oxide and tungsten oxide.

18. The measurement system according to claim 17, wherein the light radiation means irradiates anyone of the treatment substrate containing silicon, the treatment substrate containing silicon and oxygen, and the treatment substrate containing silicon and **nitrogen** with the light.

AN 1998:159774 USPATFULL|
TI Measurement system and measurement method|
IN Katsumata, Ryota, Yokohama, Japan
Hayasaka, Nobuo, Yokosuka, Japan
Yasuda, Naoki, Yokohama, Japan
Miyajima, Hideshi, Yokohama, Japan
Higashikawa, Iwao, Tokyo, Japan
Hotta, Masaki, Sagamihara, Japan
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)
PI US 5851842 19981222
AI US 1997-857360 19970515 (8)
PRAI JP 1996-121918 19960516
JP 1997-65147 19970318
DT Utility|
FS Granted|
EXNAM Primary Examiner: Powell, William|
LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.|
CLMN Number of Claims: 22|
ECL Exemplary Claim: 11|
DRWN 24 Drawing Figure(s); 13 Drawing Page(s)|
LN.CNT 1731|
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L2 ANSWER 1 OF 9 USPATFULL
SUMM An inter-layer insulation film is formed, using an insulation film of a **low dielectric constant,** contact holes and
trenches are made by dual damascene type plasma is used when the lower layer is metal such. . .
DETD In the above description, an inter-layer insulation film should be an insulation film with a **low dielectric**
constant. Contact holes and trenches should be formed by dual damascene type. RF plasma is used for the cleaning process when. . .

DETD In the above description, an inter-layer insulation film should be an insulation film with a **low dielectric**
constant. Contact holes and trenches should be formed by dual damascene type. RF plasma is used for the cleaning process when. . .

DETD In the above process, reaction gas such as helium (He), hydrogen (H.sub.2) or **argon** (Ar) may be used for **plasma**
treatment process, and the process is performed within 100 W through 500 W. A DLI, a CEM or a vaporizer of. . .
AN 2002:29338 USPATFULL
TI Method of forming a copper wiring in a semiconductor device
IN Pyo, Sung Gyu, Ichon-shi, KOREA, REPUBLIC OF
Kim, Heon Do, Kunpho-shi, KOREA, REPUBLIC OF
PA Hyundai Electronics Industries Co., Ltd., Ichon, KOREA, REPUBLIC OF (non-U.S. corporation)
PI US 6346478 B1 20020212
AI US 2000-488521 20000121 (9)
PRAI KR 1999-13008 19990413
DT Utility
FS GRANTED
EXNAM Primary Examiner: Niebling, John F.; Assistant Examiner: Gurley, Lynne
LREP Pennie & Edmonds LLP
CLMN Number of Claims: 81
ECL Exemplary Claim: 1
DRWN 4 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 1232
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L2 ANSWER 2 OF 9 USPATFULL
SUMM . . . the outside barrier layer, reducing its effectiveness. Fourth, to control wettability of the barrier layers, the Hirao technique describes an **argon-plasma treatment,**
another time-consuming step that further impairs its practicality.
DETD . . . The preferred embodiment uses a porous silicon dioxide. (For details on forming this material, see U.S. Pat. No. 5,470,801 entitled
"
Low Dielectric Constant Insulation Layer for
Integrated Circuit Structure and Method of Making Same" which is incorporated herein by reference.) Hole 28a is. . .
AN 2001:144289 USPATFULL
TI Methods for making copper and other metal interconnections in
integrated
circuits
IN Ahn, Kie Y., Chappaqua, NY, United States
Forbes, Leonard, Corvallis, OR, United States
PA Micron Technology, Inc. (U.S. corporation)
PI US 2001017424 A1 20010830
AI US 2001-817447 A1 20010326 (9)

RLI Division of Ser. No. US 1998-32197, filed on 27 Feb 1998, GRANTED, Pat. No. US 6211073
DT Utility
FS APPLICATION
LREP SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.O. BOX 2938, MINNEAPOLIS, MN, 55402
CLMN Number of Claims: 38
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 502
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L2 ANSWER 3 OF 9 USPATFULL
SUMM . . . the outside barrier layer, reducing its effectiveness. Fourth, to control wettability of the barrier layers, the Hirao technique describes an **argon-plasma treatment,** another time-consuming step that further impairs its practicality.
DETD . . . The preferred embodiment uses a porous silicon dioxide. (For details on forming this material, see U.S. Pat. No. 5,470,801 entitled " **Low Dielectric Constant** Insulation Layer for Integrated Circuit Structure and Method of Making Same" which is incorporated herein by reference.) Hole 28a is. . .
AN 2001:47947 USPATFULL
TI Methods for making copper and other metal interconnections in integrated circuits
IN Ahn, Kie Y., Chappaqua, NY, United States
Forbes, Leonard, Corvallis, OR, United States
PA Micron Technology, Inc., Boise, ID, United States (U.S. corporation)
PI US 6211073 B1 20010403
AI US 1998-32197 19980227 (9)
DT Utility
FS Granted
EXNAM Primary Examiner: Smith, Matthew; Assistant Examiner: Lee, Calvin
LREP Schwegman, Lundberg, Woessner & Kluth, P.A.
CLMN Number of Claims: 44
ECL Exemplary Claim: 1
DRWN 11 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 692
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L14 ANSWER 5 OF 20 USPATFULL

AB . . . need for an additional deposited layer. In one aspect, the invention treats an exposed surface of carbon-containing material, such as **silicon carbide**, with an inert gas plasma, such as a **helium** (He), **argon** (Ar), or other inert gas plasma, or an oxygen-containing plasma such as a nitrous oxide (N.sub.2O) plasma. Other carbon-containing materials can include organic polymeric materials, amorphous carbon, amorphous fluorocarbon, carbon containing oxides, and other carbon-containing materials. The **plasma treatment** is preferably performed in situ following the deposition of the layer to be treated. Preferably, the processing chamber in which in situ deposition and **plasma treatment** occurs is configured to deliver the same or similar precursors for the carbon-containing layer(s). However, the layer(s) can be deposited. . .

SUMM . . . The present invention relates generally to the fabrication of integrated circuits on substrates. More particularly, the invention relates to a **plasma treatment** of carbon-containing layers, such as **silicon carbide**, to enhance adhesion to an adjacent layer and to minimize oxidation of the carbon-containing layer.

SUMM . . . the invention treats an exposed surface of carbon-containing material, such as SiC, with an inert gas plasma, such as a **helium** (He), **argon** (Ar), or other inert gas plasma, or an oxygen- containing plasma such as a nitrous oxide (N.sub.2O) plasma. Other carbon-containing. . .

DETD . . . the trimethylsilane flowing at a preferable rate of about 50 to about 200 sccm./ Preferably, a noble gas, such as **helium** or **argon**, is also flown into the chamber at a rate of about 200 to about 1000 sccm. The chamber pressure is. . .

DETD . . . contained a similar composition. The He plasma was used without the substantial presence of other gases including oxygen, hydrogen, and/or **nitrogen**. To the extent that any oxygen, hydrogen, and/or **nitrogen** was present in the He gas plasma, the presence of such gases was negligible.

DETD . . . of the various layers, the oxide on the conductor can be exposed to a plasma containing a reducing agent of **nitrogen** and hydrogen, such as ammonia, to reduce the oxide.

DETD . . . dielectric layer, the flow rate of silicon tetrafluoride, commonly used for a FSG deposition, may be reduced while increasing the **helium** or **argon** flow to create a smooth transition from the dielectric layer to the SiC layer. The flexibility in the transition is. . .

CLM What is claimed is:

. . . 3, wherein exposing the carbon-containing layer to the treatment plasma comprises exposing the layer in the substantial absence of oxygen, **nitrogen**, and hydrogen containing gases.

AN 2002:105760 USPATFULL|

TI PLASMA TREATMENT TO ENHANCE ADHESION AND TO MINIMIZE OXIDATION OF CARBON-CONTAINING LAYERS|

IN HUANG, JUDY, LOS GATOS, CA, UNITED STATES

PI US 2002054962 A1 20020509

AI US 1999-336525 A1 19990618 (9)

DT   Utility|
FS   APPLICATION|
LREP   PATENT COUNSEL, APPLIED MATERIALS INC, LEGAL AFFAIRS DEPARTMENT, P O
BOX
        450A, SANTA CLARA, CA, 95052|
CLMN   Number of Claims: 23|
ECL   Exemplary Claim: 1|
DRWN   3 Drawing Page(s)|
LN.CNT 718|
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

1/23 102

> d kwic bib total

L4 ANSWER 1 OF 6 USPATFULL

SUMM . . . employ interposed between the patterns of patterned microelectronic conductor layers when fabricating microelectronic fabrications microelectronic dielectric layers formed of comparatively **low dielectric constant** dielectric materials having dielectric constants in a range of from about 2.0 to about 4.0. For comparison purposes, microelectronic dielectric. . . .

SUMM Microelectronic dielectric layers formed of comparatively **low dielectric constant** dielectric materials are desirable in the art of microelectronic fabrication formed interposed between the patterns of patterned microelectronic conductor layers. . . .

SUMM Of the comparatively **low dielectric constant** dielectric materials which may be employed for forming microelectronic dielectric layers within microelectronic fabrications, carbon doped silicon containing dielectric materials,. . . .

SUMM . . . the first object of the present invention, wherein the carbon doped silicon containing dielectric layer is formed with a comparatively **low dielectric constant** while simultaneously having enhanced adhesion with respect to an additional microelectronic layer formed thereupon.

SUMM . . . containing dielectric layer within a microelectronic fabrication, wherein the carbon doped silicon containing dielectric layer is formed with a comparatively **low dielectric constant**, while simultaneously having an enhanced adhesion of an additional microelectronic layer formed thereupon.

DETD . . . containing dielectric layer within a microelectronic fabrication, wherein the carbon doped silicon containing dielectric layer is formed with a comparatively **low dielectric constant**, while simultaneously having enhanced adhesion with respect to an additional microelectronic layer formed thereupon.

DETD . . . object, it has been determined experimentally that comparatively mild conditions employed within the oxidizing plasma 18 will preserve the desirably **low dielectric constant** dielectric constant properties of the blanket carbon doped silicon oxide dielectric layer 16 when forming therefrom the oxidizing plasma treated. . . .

DETD . . . patterned carbon doped silicon oxide dielectric layers 16a', 16b' and 16c' are formed while preserving a desirably low and comparatively **low dielectric constant** of the carbon doped silicon containing dielectric material from which is formed the blanket carbon doped silicon oxide dielectric layer. . . .

DETD . . . silicon oxide dielectric layers were then exposed to various plasma treatments which included: (1) a low temperature nitrous oxide and **helium plasma treatment** at a temperature of about 30 degrees centigrade for a time period of either one minute or two minutes, while. . . area and a nitrous oxide flow rate of about 200 standard cubic centimeters per minute (sccm); (3) a high temperature **helium plasma treatment** at a temperature of about 400 degrees centigrade for a time period of about one minute, while also employing a. . . a helium flow rate of about 500 standard cubic centimeters per minute; (4) a high. temperature 20 percent oxygen in **helium plasma treatment** at a temperature of about 400 degrees centigrade for a time period of about 30 seconds, while also employing a. . . .

AN 2002:144199 USPATFULL
TI Soft plasma oxidizing plasma method for forming carbon doped silicon containing dielectric layer with enhanced adhesive properties
IN Li, Lain-Jong, Hualien, TAIWAN, PROVINCE OF CHINA
Bao, Tien-I, Hshin-Chu, TAIWAN, PROVINCE OF CHINA
Lin, Cheng-Chung, Taipei, TAIWAN, PROVINCE OF CHINA
Jang, Syun-Ming, Hsin-Chu, TAIWAN, PROVINCE OF CHINA
PA Taiwan Semiconductor Manufacturing Co., Ltd, Hsin Chu, TAIWAN, PROVINCE OF CHINA (non-U.S. corporation)
PI US 6407013 B1 20020618
AI US 2001-761422 20010116 (9)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Ghyka, Alexander G.
LREP Tung & Associates
CLMN Number of Claims: 13
ECL Exemplary Claim: 1
DRWN 5 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 794
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L4 ANSWER 2 OF 6 USPATFULL
SUMM The present invention relates generally to fabricating semiconductor devices and specifically to methods of forming **low dielectric constant** (low-k) materials used in fabricating semiconductor devices.
SUMM U.S. Pat. No. 5,661,093 to Ravi et al. describes a method for depositing a halogen-doped oxide film having a **low dielectric constant** that is resistant to outgassing of the halogen dopant and moisture absorption, and also retains these properties during subsequent processing. . . .
SUMM Accordingly, it is an object of the present invention to provide a method of forming CVD **low dielectric constant** material having improved crack resistance.
SUMM . . . object of the present invention is to provide a method of forming up to and over 3 .mu.m thick CVD **low dielectric constant** material having improved crack resistance.
SUMM Yet another object of the present invention is to provide a method of forming improving the crack resistance of CVD **low dielectric constant** material having without sacrificing the **low dielectric constant** characteristic of the material.
DETD The CVD low-k SiOCN film made in accordance with the present invention also maintains the Prior CVD low-k film's **low dielectric constant** characteristics. For example, in the case of BD, Prior BD has a final dielectric constant after processing of about 3.22. . . .
CLM What is claimed is:
7. The method of claim 1, wherein said stabilization treatment of said final deposited film includes a **helium plasma treatment** at from about 15 to 19.degree. C.

15. The method of claim 10, wherein said stabilization treatment of said final deposited film includes a **helium plasma treatment** of about 15 to 19.degree. C.

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AN      2002:81415  USPATFULL|
TI      Method to improve the crack resistance of CVD low-k dielectric constant
        material|
IN      Lin, Cheng Chung, Taipei, TAIWAN, PROVINCE OF CHINA
        Jeng, Shwang Ming, Hsin-Chiu, TAIWAN, PROVINCE OF CHINA
        Li, Lain Jong, Hwa-Liang, TAIWAN, PROVINCE OF CHINA
PA      Taiwan Semiconductor Manufacturing Company, Hsin-Chu, TAIWAN, PROVINCE
        OF CHINA (non-U.S. corporation)
PI      US 6372661          B1   20020416
AI      US 2000-617011           20000714 (9)
DT      Utility|
FS      GRANTED|
EXNAM   Primary Examiner: Everhart, Caridad; Assistant Examiner: Lee, Jr.,
        Granvill D|
LREP    Saile, George O., Ackerman, Stephen B., Stanton, Stephen G.|
CLMN    Number of Claims: 32|
ECL     Exemplary Claim: 1|
DRWN    3 Drawing Figure(s); 3 Drawing Page(s)|
LN.CNT 563|
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
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2 ANSWER 3 OF 7 USPATFULL

DETD Suitable dielectric or passivation materials include, without limitation, any dielectric capable of passivating a **SiC** substrate. Preferred dielectrics include oxides, nitrides, oxynitrides, and mixtures thereof. Suitable oxides include, without limitation, thermally grown or deposited oxides,. . . low temperature thermal oxides (LTO), triethylorthosilane formed oxides (TEOS), and mixtures or combination thereof. Other suitable dielectrics include, without limitation, **deposited silicon nitride,** oxynitride, and thermally-formed nitrided silicon oxide.

AN 2002:81775 USPATFULL

TI Passivated silicon carbide devices with low leakage current and method of fabricating

IN Alok, Dev, Danbury, CT, United States
Arnold, Emil, Chappaqua, NY, United States

PA Philips Electronics North America Corporation, New York, NY, United States (U.S. corporation)

PI US 6373076 B1 20020416

AI US 1999-455663 19991207 (9)

DT Utility

FS GRANTED

EXNAM Primary Examiner: Flynn, Nathan; Assistant Examiner: Forde, Remmon R.

CLMN Number of Claims: 20

ECL Exemplary Claim: 1

DRWN 8 Drawing Figure(s); 5 Drawing Page(s)

LN.CNT 554

CAS INDEXING IS AVAILABLE FOR THIS PATENT.